MAXIM Engineering Journal

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News Briefs

MAXIM REPORTS RECORD REVENUES, EARNINGS, AND OPERATING INCOME FOR THE FIRST QUARTER OF FY96

Maxim Integrated Products, Inc., reported record net revenues of $96.4 million for the first quarter of fiscal 1996 ending September 30, 1995, compared to $52.0 million for the same period a year ago. This represents an 85.4% increase in net revenues from the same quarter a year ago and a 26.9% gain over Q495. Net income was $22.6 million (or $0.64 per share) for the quarter, compared to net income of $8.3 million (or $0.26 per share) for the same quarter in fiscal 1995. Operating income was a record 36.1% of net revenues, compared to 23.7% for Q195. Annualized return on equity increased to 46.5% for Q1 compared to 25.2% for fiscal 1995.

Cost of sales in the first quarter results included approximately $3.5 million in costs related to the Company's continued expansion of its Beaverton manufacturing facility.

During the quarter, cash and short-term investments increased by $9.5 million. The Company purchased over $8.7 million in capital equipment and also repurchased approximately $11.8 million of its common stock. Inventories were at a record low level of 35 days of cost of sales, representing a substantial improvement over the Q495 level of 56 days. Accounts receivable levels were at 51 days of revenues, reflecting the higher level and timing of revenues for the quarter. Depreciation expense for Q196 was $3.0 million, an increase of 26% over Q195. Wafer fabrication capacity increased 100% during the same period.

Jack Gifford, Chairman, President, and CEO commented, "Maxim's pioneering contribution to portability in a wide variety of electronic products has resulted in broad growth of international acceptance of Maxim as the glamour brand in analog ICs. Also, as Maxim's customers continue to reduce their time from design to market, the initial sales for Maxim's products have accelerated. Both effects have contributed to increased product acceptance. Average third year sales for Maxim products are now $500,000 compared to $200,000 just 6 years ago.

"For the first time in several quarters, factory shipments for the first quarter exceeded what we believe to be the current end market consumption for those products. Maxim expects this trend to continue through fiscal 1996 as production capacity continues to increase.

"We are pleased with our factory's performance with respect to the capacity expansion plan we outlined at the end of last quarter. We estimate that our increased capacity will enable us to ship over 75% more units in fiscal 1996 than we did in fiscal 1995. This compares favorably with fiscal 1995 unit shipments, which were 48% over those for fiscal 1994. We are continuing to expand our Beaverton production facility with a goal of increasing production levels in Q496 by as much as 100% over Q296 levels. We have also embarked on a plan to build a 115,000-square-foot assembly and test facility at the Gateway Industrial Park in the Philippines to further increase our back end capacity."

Gifford continued, "We are pleased to see that Maxim has once again been selected by *Forbes* to be on the Honor Roll of the '200 Best Small Companies in America.' Maxim is one of only 11 companies to be on the *Forbes* 200 List at least 6 times since 1980."

Maxim's analog switches and multiplexers lead the industry in low voltage, low leakage, and high performance

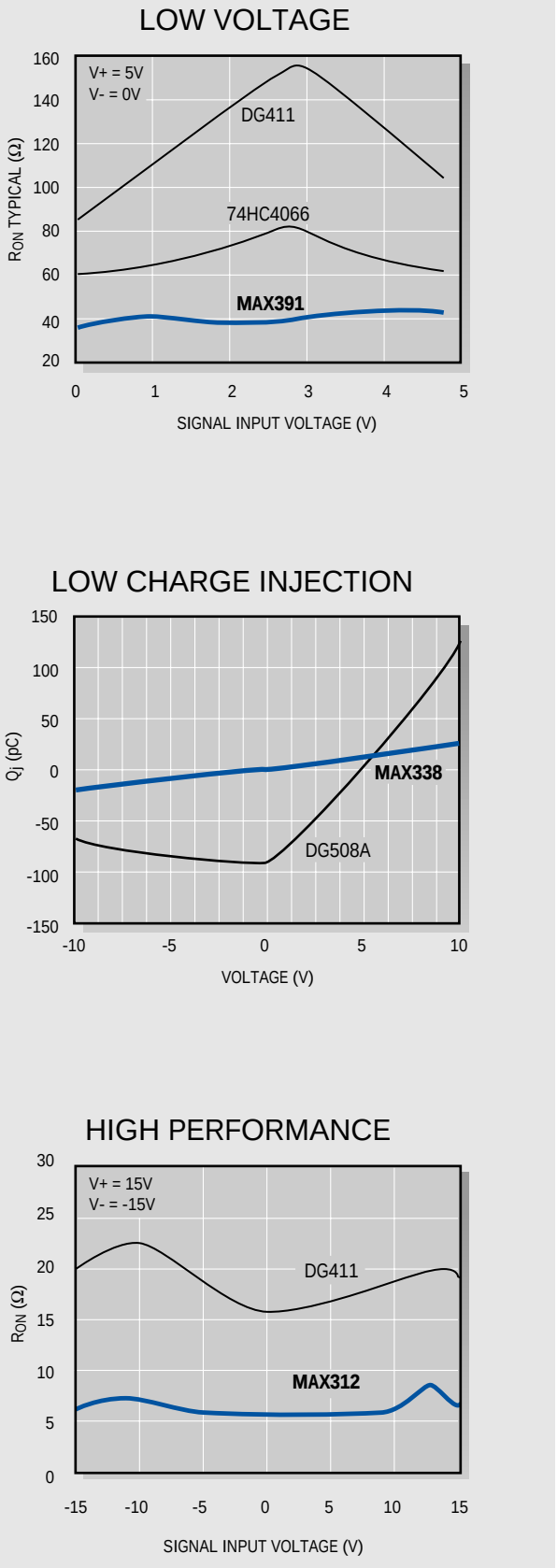
For more than twenty-five years, monolithic analog switches and multiplexers have served as fundamental building blocks in analog circuit design. Integrated-circuit switches have replaced most signal-switching circuits made from discrete component transistors and logic-level shifters. Equally important, IC switches have continued to benefit from process and design improvements that reduce supply voltage, power consumption, on-resistance, charge injection, and switching time.

Switch and multiplexer architectures have not changed in many years, but the constant demand for lower supply voltage, better precision, and tighter spec tolerance obliges manufacturers to persevere with development—if only to achieve incremental performance improvements. To appreciate what the latest switch and multiplexer products can do, consider the components integrated on a typical chip.

Circuit blocks

For most of today's analog switches, the actual switching element is a pair of metal-oxide-semiconductor field-effect transistors (MOSFETs). Unlike bipolar transistors, MOSFETs can handle bidirectional drain-to-source channel currents. Moreover, a voltage-controlled MOSFET is free of the error caused by base-to-emitter currents in a bipolar transistor. MOSFET switches exhibit on-resistance, but no dc offset.

In switching applications, enhancement-mode MOSFETs—offering better characteristics and easier fabrication—are preferable to depletion types. Enhancement-mode types are self-isolating, with drain and source regions formed in a single diffusion step. Because all active regions are reverse-biased with respect to each other and the substrate, adjacent devices on the



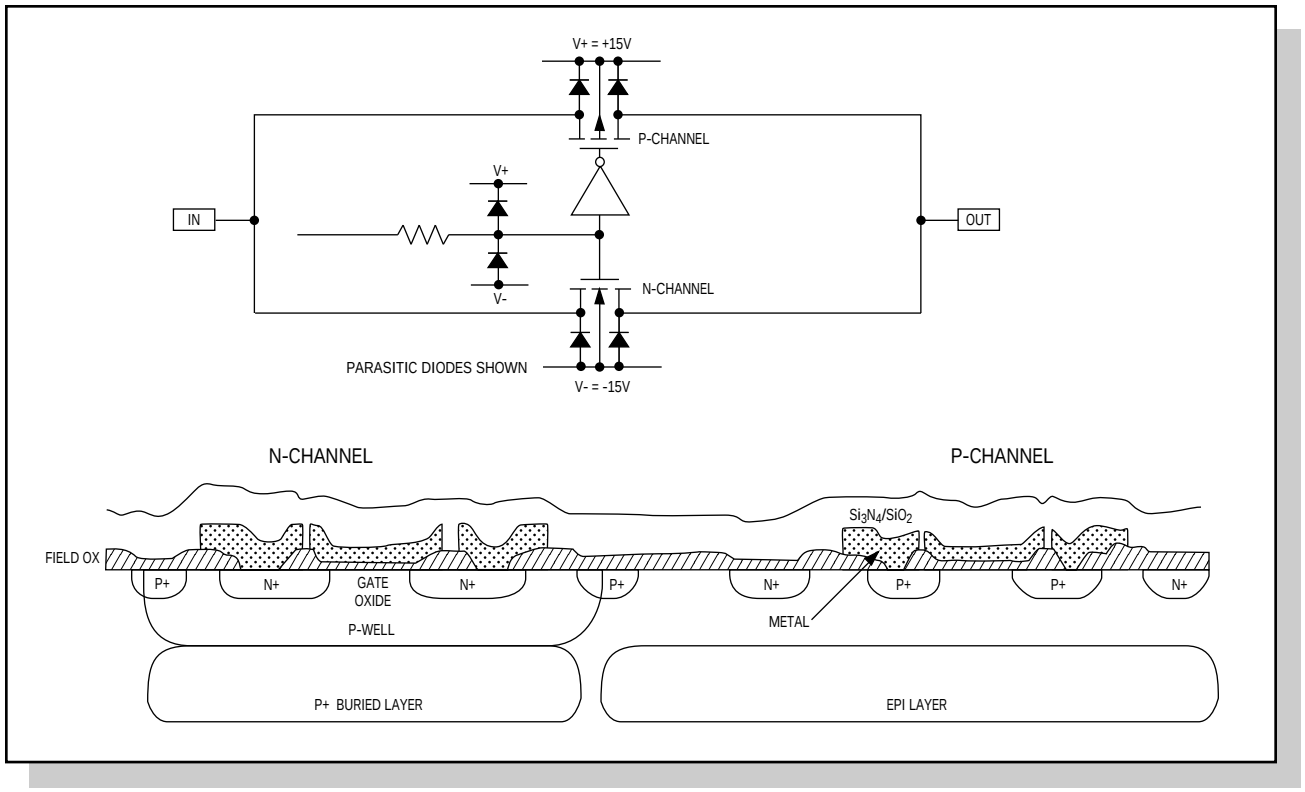


Figure 1. This cross section of the two MOSFETs in an IC transmission gate shows parasitic diodes tied to the supply rails.

same substrate are electrically isolated without recourse to dielectric isolation or other special techniques. The MOSFET's insulated gate minimizes the effect of dc control voltage on the signal channel.

A single n-channel or p-channel enhancement-mode MOSFET can serve as an analog switch, but its on-resistance will vary considerably with signal voltage. Connecting an n-channel and p-channel device in parallel—the almost universal configuration for CMOS analog switches—greatly reduces this variation. Complementary gate-drive signals turn the two devices on or off simultaneously. **Figure 1** shows the cross section of an n-channel and p-channel device as they appear in a monolithic structure.

The need for fault-tolerant switching has brought about a major exception to the parallel-FET arrangement. By connecting an n-channel, a p-channel, and an n-channel device in series, you can implement a switch channel that turns off automatically when the analog signal approaches either power rail (see *Selection Guides—Fault Protection*).

On-resistance characteristics are the key to understanding these major switch architectures. On-resistance in either device type alone (p or n) is a strong function of the gate-source bias. But connecting the devices in parallel yields an on-resistance that is relatively constant for most of the analog-signal range (**Figure 2**). Processing improvements have repeatedly lowered the gate-source threshold, from that of metal-gate technology (2.5V to 5V) to that of silicon-gate technology (about 900mV).

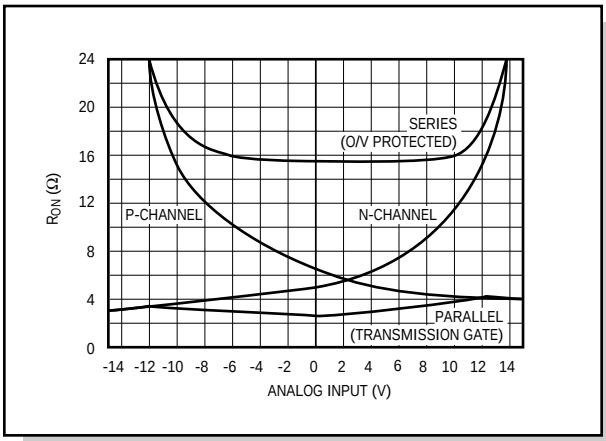


Figure 2. The on-resistance of an n-channel or p-channel MOSFET by itself is quite large at one extreme of the V_{IN} range, but in parallel, their composite resistance remains relatively flat. R_{ON} for an overvoltage-protected switch is approximately six-times higher because the switching element has three MOSFETs in series.

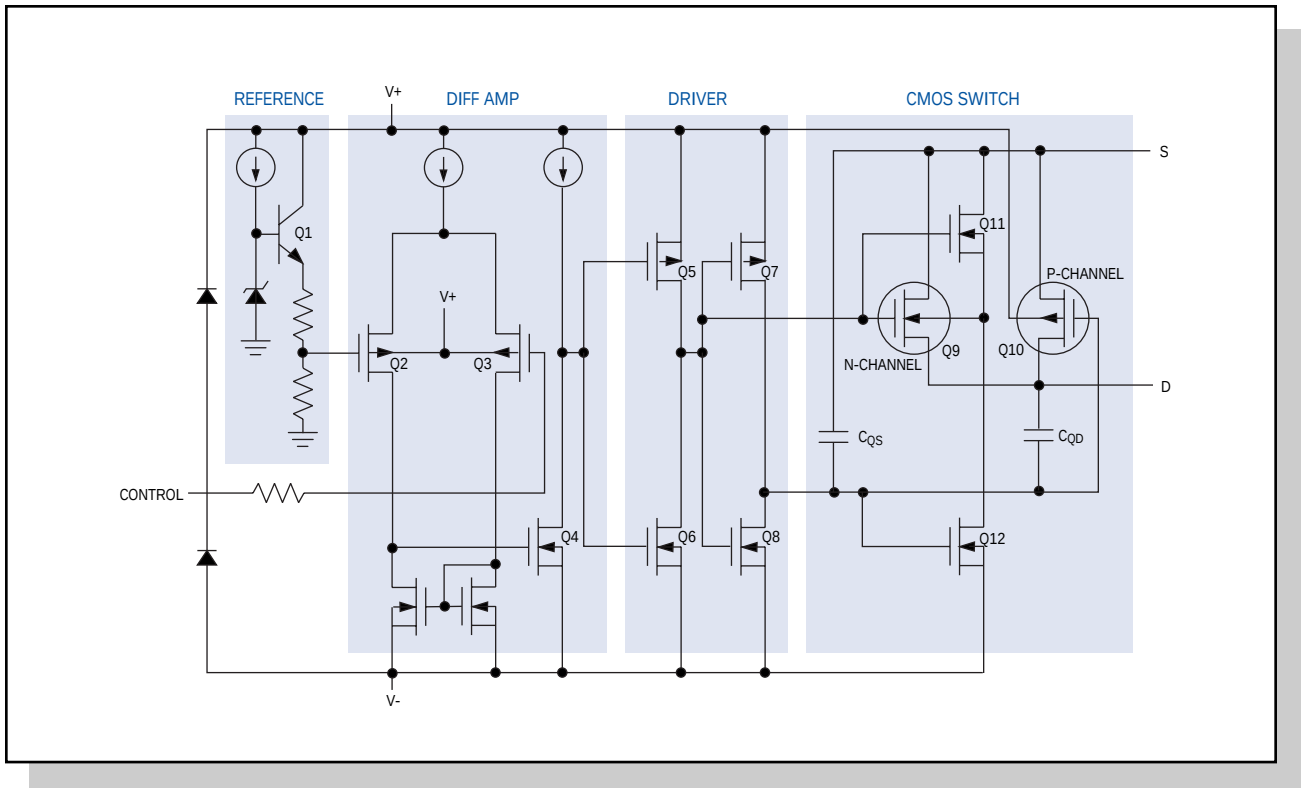


Figure 3. The gate-drive circuitry in this analog switch derives complementary ±15V signals from a single logic level at V_{IN}.

Adding level translators and complementary gate-drive signals lets you control the switch with an applied logic level (**Figure 3**). Applied to one input of the comparator Q2/Q3, this external level establishes an internal logic state (high or low) with respect to a reference voltage connected to the comparator's other input. The comparator outputs then drive complementary inverting buffers (Q5–Q8) that provide the phase and current gain necessary to charge and discharge gate capacitance in the switching MOSFETs Q9 and Q10.

To turn the switch on, connect the n-channel gate to the positive rail and the p-channel gate to the negative rail. One FET is always on as the source connection swings to either extreme of the analog range. The switch can function with its FET body connections tied directly to the supply rails, but the Q11 and Q12 connections shown enhance performance by lowering the switch leakage and reducing the modulation of on-resistance.

Q11 and Q12 form a "body snatcher" for the n-channel switching FET. When the switch is on, Q11 connects the body of Q9 to its source, eliminating modulation of the channel by ensuring a constant source-to-body voltage. When the switch is off, Q12 improves off isolation and leakage by connecting the body of Q9 to the negative rail.

Body-snatcher improvements are not without side effects. If Q11 and Q12 turn on together, even for an instant, they momentarily connect the switch source to the negative rail, producing negative charge injection and lengthening the on/off times. The chip design ensures that these transistors are never on at the same time.

When the switch changes state, the Q5/Q6 and Q7/Q8 inverters produce gate-drive waveforms with sharp edges, which pass through the Q9/Q10 gate-source and gate-drain capacitances and into the analog signal channel. If left uncorrected, the resulting charge-injection spikes can overload downstream circuitry, lengthen settling times, and produce annoying "splats" in an audio loudspeaker. Capacitors C_{QS} and C_{QD} enhance performance by compensating for this charge injection at the source and drain connections.

If the gate-source capacitances for equivalent n- and p-channel devices were equal, the IC designer might cancel charge-injection effects by ensuring truly complementary waveforms at the gates of Q9 and Q10. But these capacitances are not equal: the conductance of n-type material is 2.5 to 2.8 times larger than that of p-type material. For equal on-resistances, therefore, the p-channel's size and gate-source capacitance must be 2.5 to 2.8 times larger than that of the n-channel device.

Thus, capacitors C_{QS} and C_{QD} compensate for the geometric imbalance between Q9 and Q10. Each capacitor is a binary-weighted array, trimmed at the mask level for a particular signal voltage (usually 0V in a dual-rail circuit) to minimize charge injection at the source and drain terminals. The complication is that the gate-source and gate-drain capacitances (which are produced by reverse-biased diode junctions) vary with the signal voltage. This effect requires additional, dynamic compensation in the form of extra diodes or a dummy switch.

On-switch (static) modeling

Successful design with analog switches and multiplexers calls for an understanding of parasitic and non-ideal characteristics in the basic switch architecture. Models for the on and off states of a switch let you study its static and dynamic effects on a system. Static (steady-state) effects include on and off capacitances, voltage-swing limits, leakage current, transmission loss, bandwidth, and crosstalk. Dynamic effects include on and off switching times, settling time, and propagation delay.

For the steady-state on condition, the Figure 3 switch can be modeled as in **Figure 4a** and simplified as in **Figure 4b**. First, the power-supply limits determine the analog signal range. If a signal excursion exceeds either power rail, the associated parasitic diode will conduct and inject current into the substrate, producing problems such as gross output distortion and increased leakage in the adjacent switches.

At some level of parasitic-diode current, the IC can latch up and destroy itself, so you should limit supply currents per the Absolute Maximum Ratings. On the other hand, if large signals are predictable in your application, consider a fault-tolerant structure such as the series-FET type mentioned earlier, which prevents current flow during overvoltage conditions.

The parasitic diodes in question also cause most of the unwanted leakage specified for an analog switch or multiplexer. In a perfect switch, the diodes would be matched; for equal reverse voltages, the net leakage into and out of the source and drain terminals would be zero. Actual leakages are not matched, of course, so a data sheet must specify the net difference current for each case (see *Selection Guides—Low Leakage*).

To simplify leakage tests during production, manufacturers measure the total on-state leakage at the drain terminal. This current flows through the on-resistance and produces offset-voltage errors, so a high signal-source impedance demands a low switch leakage.

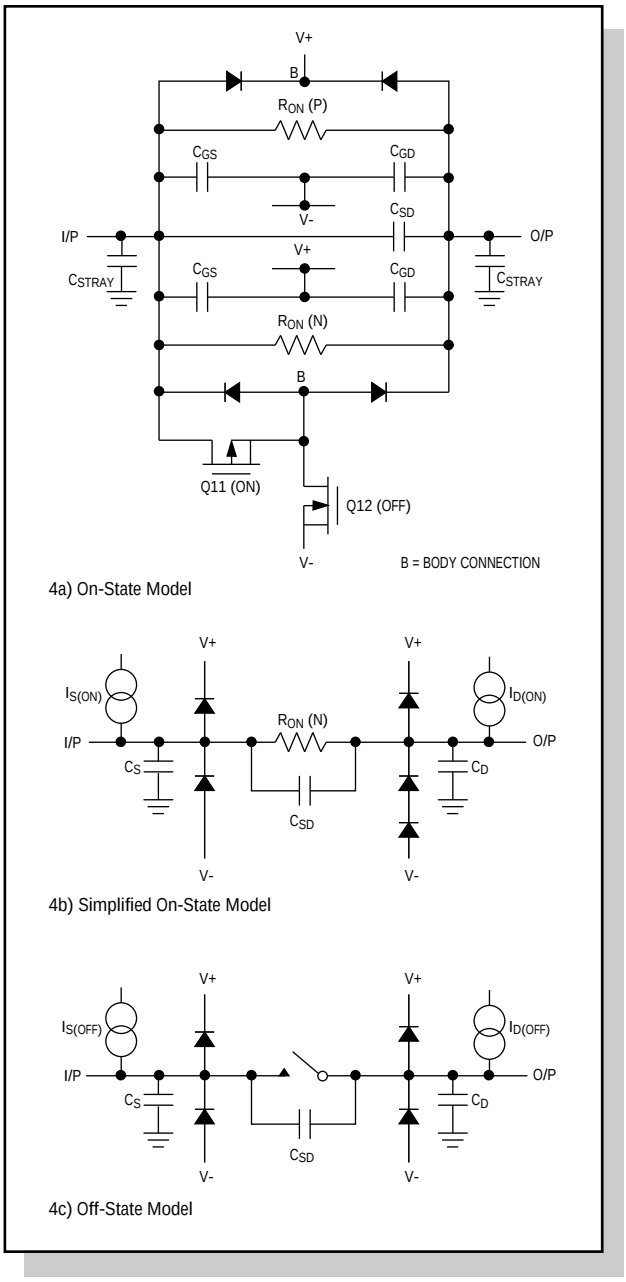


Figure 4. These lumped-parameter models of an analog switch let you estimate the effect of its static and dynamic operation.

Moreover, the analog signal modulates this leakage by varying the reverse bias across the parasitic diodes. To ensure worst-case measurements, the data sheet specifies leakage in the presence of a signal voltage near the supply rails, which subjects the diodes to a maximum imbalance in reverse bias.

For small-signal low-frequency conditions, you can define input-to-output transmission loss (L_{TRANS}, in dB) in terms of on-resistance and the output load resistance R_L:

$$L_{TRANS} = 20\log[R_L / (R_L + R_{ON})].$$

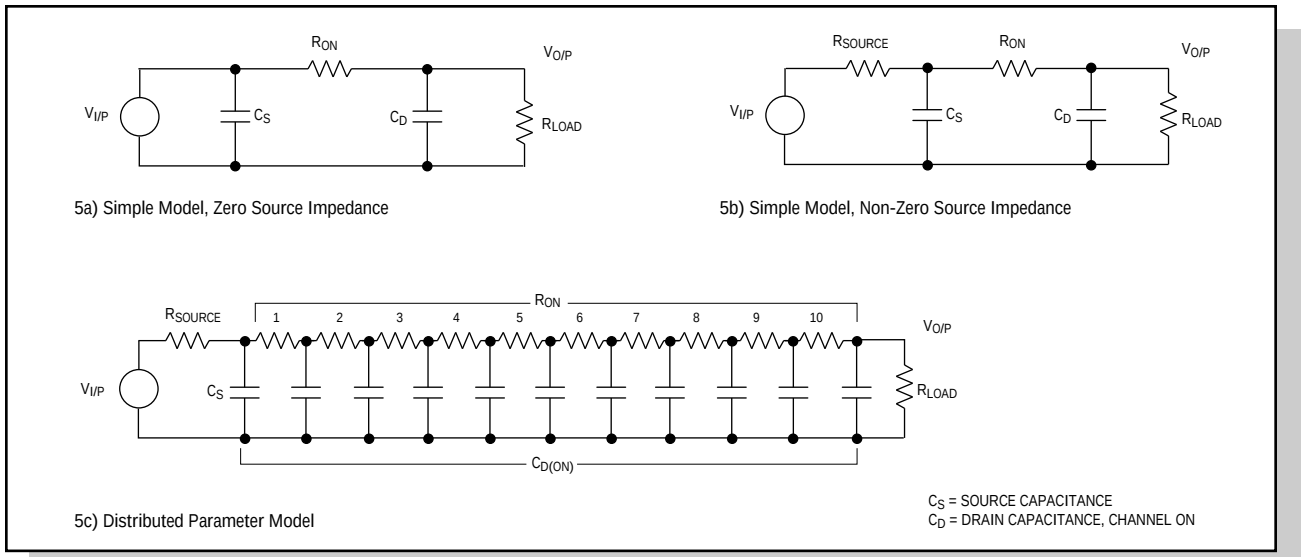


*Figure 5. A simple switch-bandwidth model (**a**) is made more accurate by adding source impedance (**b**), and more accurate still by representing the distributed R_{ON} and CD as a cascade of sections (**c**).*

R_{ON} is proportional to absolute temperature, so L_{TRANS} is also a function of temperature. Small signal is defined as small enough to avoid modulation of the on-resistance (100mV or less). Larger signals, up to those encompassing the full dynamic range of the switch, produce a distortion error (D, in percent) due to the change of on-resistance with analog signal swing:

$$D = 100\Delta R_{ON} / R_L.$$

Thus, to achieve lowest distortion when operating in the voltage mode, you must minimize ΔR_{ON} and maximize R_L. The specifications for recent products help you implement this goal: MAX3xx switches and multiplexers, for example, are the first to provide—in addition to static on-resistance—separate specs for channel-to-channel matching and for signal swing vs. dynamic variation about the static value (see *Selection Guides—Low On-Resistance*).

"The lower the better" applies for on-resistance in most applications. An excellent way to produce low-on-resistance switches from standard parts is to parallel the switch sections in a single IC. Using switches from the same die assures a good match in the logic propagation delays. For example, the MAX351 (a precision quad SPST switch) can be wired in parallel to produce an on-resistance of 5.5Ω typical and 11.25Ω maximum, with a corresponding ΔR_{ON} of only 1.25Ω maximum. The parallel connection handles more signal current while lowering the distortion and transmission loss, but it also increases the leakage and charge injection.

Another parameter affected by on-resistance is the f_{-3dB} bandwidth. R_{ON} and C_{DRAIN} alone determine bandwidth if the switch is driven with a pure voltage source (**Figure 5a**). Otherwise, the non-zero source impedance must be accounted for (**Figure 5b**):

$$f_{-3dB} = 2\pi \frac{R_A - R_{LOAD}}{R_A + R_{ON}},$$

where $R_A = (R_{SOURCE} + R_{ON})$.

On-resistance and drain on-capacitance are not lumped parameters; both are distributed along the channel of the switching FET. For calculating actual bandwidths, these quantities are more accurately modeled as multiple sections (**Figure 5c**). This model is suitable for frequencies above 500kHz and for pulse applications in which you must calculate the signal's propagation delay through an on channel.

Off-switch (static) modeling

Off isolation and leakage are primary concerns in the off state; other parameters of interest are the signal-voltage limits, the power-supply levels and tolerances, and the input and output logic levels. You can estimate off isolation within the switch using the transmission-loss equation and a suitable switch model (**Figure 4c**). First, include in the equation the impedance effect of the drain-source capacitance, C_{SD}. Isolation depends as much on external layout as device characteristics, so when possible, you should measure its actual value in a circuit.

Off-state leakage (like on-state leakage) originates in parasitic diodes associated with the switching MOSFETs. It can be modulated by analog signals applied to the off channel, which in turn are limited by the power supplies (as for an on channel). Signal voltage beyond either supply rail causes current flow into the substrate, thereby introducing problems that depend on the current's polarity and magnitude.

Maximum supply voltages are determined by the chip's semiconductor process, and minimum values are determined by the process and the internal gate-to-source thresholds required for the switching FETs. Thus, supply rails for the standard-product DG4xx and DG5xx multiplexer families and the DG2xx, DG3xx, and DG4xx switch families may range from ±4.5V to ±22V. The single-rail limit for these products is 30V. Low-voltage, low-R_{ON} families such as Maxim's MAX38x and MAX39x specify ±2.7V to ±8V for dual rails and 2.7V to 16V for the single rail (see *Selection Guides—Low Voltage*).

Supply currents are specified in the data sheet, but the analog switch itself draws no current. Comprised of n- and p-channel MOSFETs in parallel, the switch is a passive device that draws no power from the supplies. Instead, supply currents are drawn by the digital interface, which converts applied logic levels to the gate-drive signals required by these parallel MOSFETs. The currents vary with applied voltage level, and they peak when the level translator is operating in its linear mode. This mode, unfortunately, occurs near the TTL levels of 0.8V and 2.4V (**Figure 6**) and produces the worst-case supply currents. If the logic voltages swing rail to rail (as when logic and analog supply voltages are equal), the supply currents drop almost to leakage levels—certainly to below 1µA.

The saturated logic drivers Q7/Q8 and Q5/Q6 provide low-impedance paths from the supply rails to the analog channel, via the gate-to-channel capacitances in Q9 and Q10. Thus, high-frequency noise can couple from each supply rail to the channel and vice versa, unless you add a decoupling network at each supply terminal. More than adequate for this purpose is 100Ω in series, shunted by 10µF in parallel with 100nF.

Most analog-switch ICs have an individual address line for each switch, up to the maximum number (of switches) practical without decoding the address on chip. This number is about four. The preferred technique for controlling more than four switches on an IC is a serial interface that reduces the pin count and provides individual control.

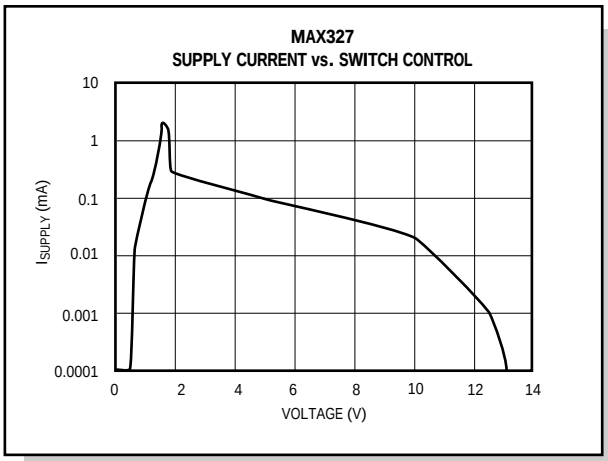


Figure 6. Input current at the V_{IN} control input of an analog switch peaks near the TTL levels of 0.8V and 2.4V.

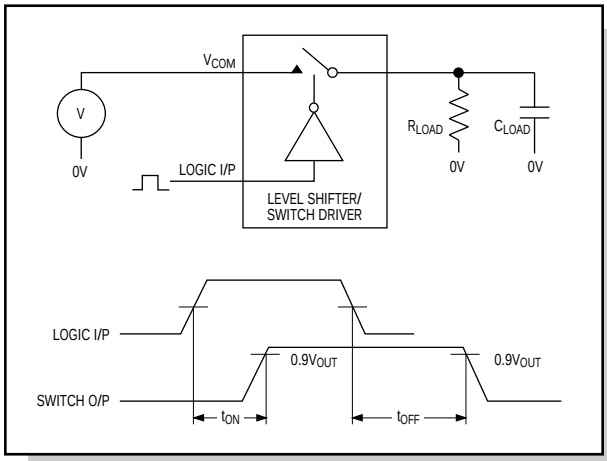


Figure 7. Internal propagation delay and an output time constant determine the on/off times for an analog switch.

For example, the MAX335—an array of eight switches in a 24-pin package—clearly illustrates the flexibility of serial control. Some such chips include digital latches with an option for transparent operation, but that arrangement may allow significant crosstalk from the active digital bus to the analog channels. If so, you may have to add an external latch to physically isolate the bus from the switches.

Dynamic switching effects

We've presented electrical models of the analog switch and linked the models to the specifications that describe a switch in the static state—on or off. Next, we consider the specifications associated with dynamic behavior; i.e., switch phenomena that occur during a change of state.

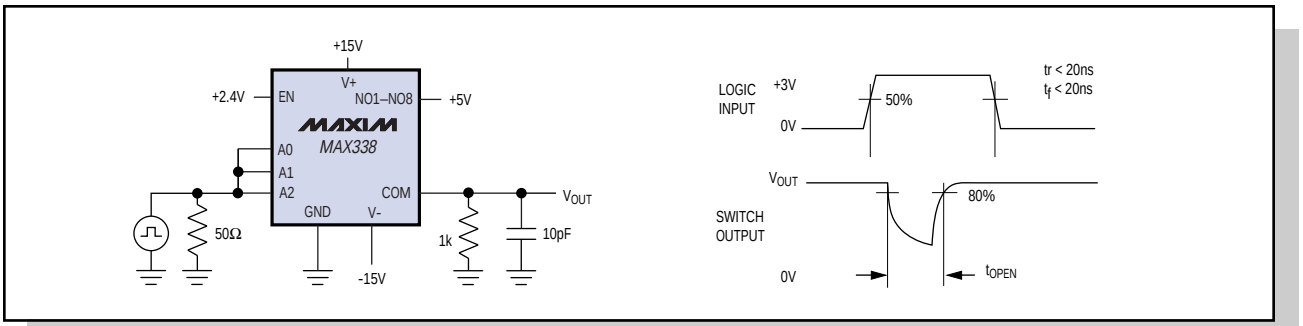


Figure 8. This test configuration enables measurement of the break-before-make interval.

Switching time, for example, is the sum of the propagation delay through the level shifter and the time it takes for load voltage to rise (or fall) to a predetermined level (**Figure 7**). Propagation delay is generally defined as the time interval from 50% of the logic transition (V_{IN}) to 90% of the output-voltage transition.

Rise and fall times are calculated from load conditions given in the data sheet. Note that manufacturers specify loads with a fast time constant to ensure that the resulting measurements are dominated by the device under test. Thus,

$$t_{ON}\text{ (switch only)} = t_{ON}\text{ (from the data sheet)} - t_{RISE(load)},$$

where $t_{RISE(load)} = (R_{ON}||R_{LOAD})C_{LOAD}[-\ln(\%\text{ error}/100)]$, and percent error is related to the percent of final value specified in the data sheet. For 90% of the final value (a standard level), the percent error is 10%. Therefore, $t_{RISE(load)} = (R_{ON}||R_{LOAD})C_{LOAD}[-\ln(0.1)] = 2.3(R_{ON}||R_{LOAD})C_{LOAD}$. Similar reasoning applies for switch off time:

$$t_{OFF}\text{ (switch only)} = t_{OFF}\text{ (from the data sheet)} - t_{FALL(load)},$$

where $t_{FALL(load)} = R_{LOAD}C_{LOAD}[-\ln(\%\text{ error}/100)]$. In this case, the fall time is specified to 10% of the final value, which again leaves 10% as the percent error. Therefore, $t_{FALL(load)} = R_{LOAD}C_{LOAD}[-\ln(0.1)] = 2.3R_{LOAD}C_{LOAD}$.

For multiple switches, the break-before-make interval guarantees (as its name implies) that two inputs cannot be shorted together. MAX338 8-channel multiplexers, for instance, guarantee minimum BBM intervals of 10ns (**Figure 8**).

Of all the dynamic specs, settling time is the most problematic to measure. Defined as the time required for V_{OUT} to settle within a specified error band centered on its final value and in response to a change from on to off or off to on, settling time depends on external source and load impedances as well as the switch on-resistance.

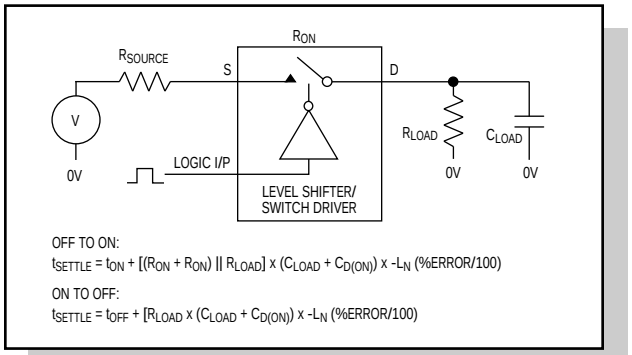


Figure 9. This simple circuit model allows an accurate estimate of settling time.

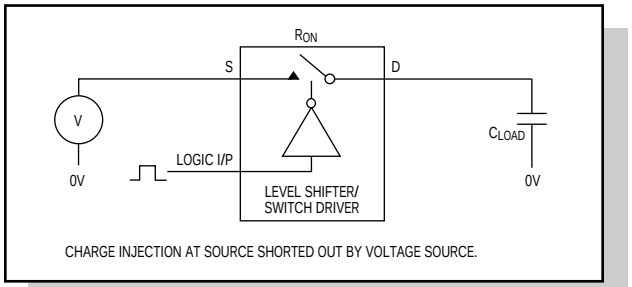


Figure 10. Low signal-source resistance shorts out the effect of charge injection at the source of the switching MOSFET.

A suitable switch model (**Figure 9**) lets you calculate the settling time. For low clocking rates at the address inputs, this model is valid to about 16 bits—a digital resolution comparable to the settling-time perturbations caused by thermal effects on the die. (Neglect of source resistance is a common oversight in these calculations.)

To support the limits guaranteed for other dynamic specifications, the digital transitions at V_{IN} are necessarily fast. The resulting voltage edges pass through the device

capacitances and inject a small charge into the analog channel, which in turn produces a small step of error voltage on the output:

$$V_{STEP} = Q / C_{LOAD}.$$

If the charge injection (Q) is in picocoulombs and C_{LOAD} is in nano-farads, V_{STEP} is in millivolts. Comparable amounts of charge are injected at the input and output. In the test setup of **Figure 10**, however, a low source resistance produces almost no voltage error due to charge injection. Voltage error due to output charge injection adds to the settling time. You can calculate that effect as before, noting that the charge-injection step decays to allow V_{OUT} to settle within the error band. To minimize charge-injection effects, many Maxim ICs require maximum rise and fall times of 20ns at the logic inputs.

Applications

Solid-state switches and multiplexers have many uses beyond the obvious applications in data acquisition and low-frequency signal processing. They can handle RF signals to 1MHz and above, for example, if the switching and isolation requirements permit. Analog switches offer the advantage of low power dissipation and a simple logic interface. Performance depends on signal current in the switching element, which (to reduce transmission loss) is generally limited to a few milliamps.

Two single-supply SPDT switches, for example, let you implement a bandwidth-filter selector for a 455kHz IF signal (**Figure 11**). Low on-resistance, matched sections, and 85dB crosstalk at 1MHz make these switches ideal for RF switching at 1MHz (or less) in portable, battery-powered systems.

For good crosstalk performance to 10MHz and beyond, consider the buffered T switch connection (**Figure 12**). This IC (the MAX383) can be connected as a single- or dual-rail T switch with low on-resistance (40Ω typical) and excellent off isolation (-80dB at 10MHz). You can add an output buffer to achieve lower distortion and lower transmission loss, but analog switches ultimately fail on crosstalk and isolation as the operating frequency increases.

On the other hand, analog switches have a level-shifting capability that enables them to switch RF signals (**Figure 13**). The applied 5V-logic signal, shifted to ±15V by the switch section, turns the RF switch on or off by biasing or reverse-biasing the two associated diodes. Current levels in the diodes depend upon their type (silicon or PIN) and the specified maximums for transmission loss and intermodulation distortion. Most

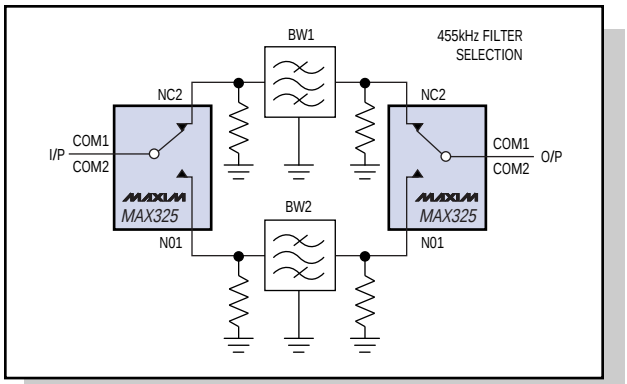


Figure 11. These single-supply SPDT switches handle frequencies as high as 1MHz.

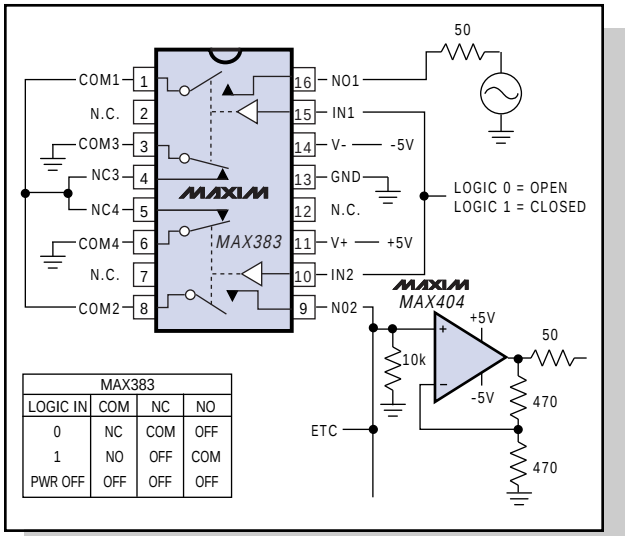


Figure 12. The buffered T switches in this application provide good performance to 10MHz and beyond.

analog switches can handle about 20mA before encountering their absolute maximum limit.

To turn the RF switch off, the SPDT switch connects the diodes to -15V. Subject to the diodes' maximum reverse-voltage rating, this configuration ensures good performance and minimum capacitance in the off state. If necessary, you can parallel two sections of the quad-SPST MAX333A to double the current delivered to the diodes.

In another type of current-controlled switch, the switching element consists of an npn- and a pnp-bipolar transistor in parallel (**Figure 14**). The output is a two-collector junction that acts like a current source (in the on state), which enables the designer to make independent choices for the values of gain and output resistance. Output resistance determines the required reverse termination, and in most applications the two resistances together are chosen for unity forward gain through the

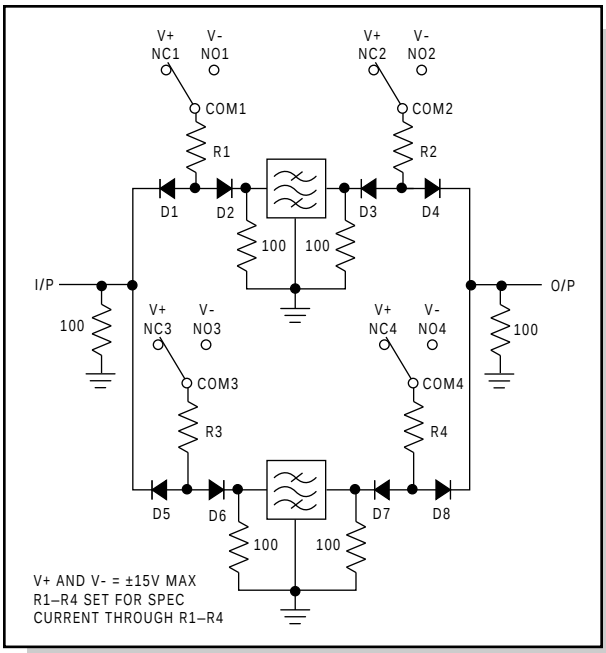


Figure 13. This quad SPDT analog switch (the MAX333A) helps implement four current-controlled RF switches.

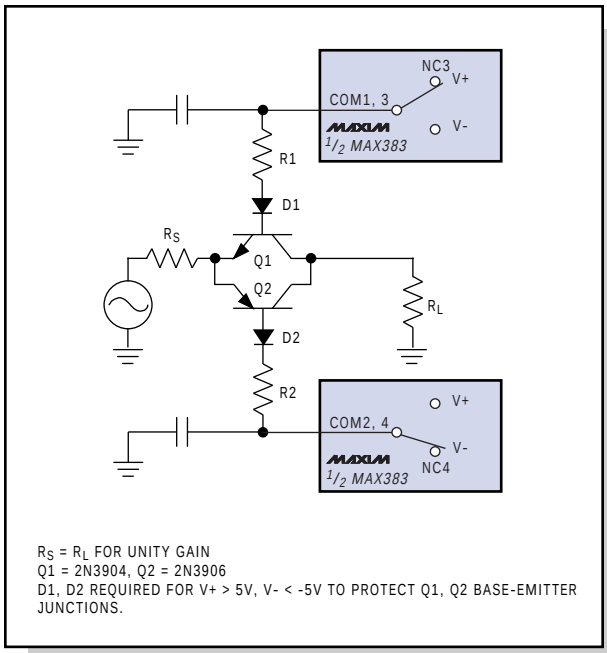


Figure 14. A dual SPDT analog switch (the MAX383) helps implement a current-controlled RF switch consisting of two bipolar transistors in parallel.

switch. D1 and D2 protect the base-emitter junctions against excessive reverse voltage in the off state.

Analog switches can also select crystals in a crystal-controlled oscillator (**Figure 15**). As before, the switch either forward-biases or reverse-biases a diode, which in turn selects or deselects the associated crystal. Supply voltages to ±8V can be switched by a MAX383 dual SPDT switch. For higher voltages, to ±18V, use a MAX411 quad SPDT switch.

Signal processing

IC switches and multiplexers are useful in circuits that select discrete levels of gain, frequency, phase, or voltage. Gain-control circuits, for example, can employ either series (**Figure 16a**) or shunt (**Figure 16b**) switching. Each approach offers advantages.

For series switching, the signal is not inverted, and the gain is independent of the switch on-resistance. Gain equals (1 + R1 / R2), where the sum R1 + R2 is constant but the relative values of R1 and R2 depend on which switch is closed. You should keep the sum low to minimize the passband zero caused by C_{STRAY} and R1||R2. A low-leakage switch with low output capacitance also minimizes this effect. You should ensure break-before-make timing to avoid an open-loop condition. Note: by substituting a 16-channel multiplexer such as the MAX306, you can select one of 16 gain levels.

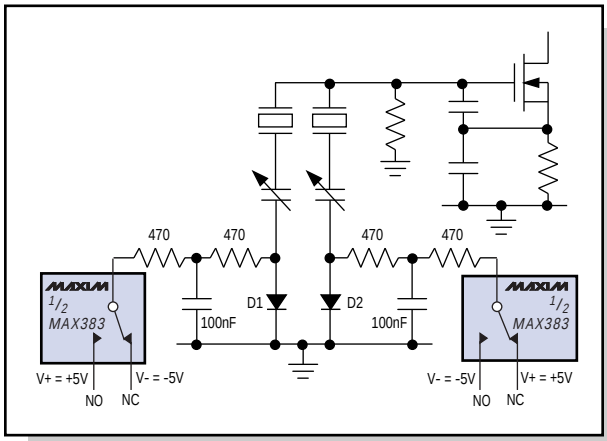


Figure 15. SPDT switches select one of two crystals in this crystal-controlled oscillator.

The shunt configuration inverts the signal. It opens all the switches at power-up (to ensure a closed loop with minimum gain) and then closes all switches except the one corresponding to the desired gain. Thus, an open switch associated with R2 (all other switches closed) produces a feedback resistance of 2R2. A closed switch at R_N produces a feedback resistance of $R_N(1 + R_N / R_{ON})$, if $R_{ON} << R_N$. Each pair of resistors isolates a switch capacitance and its effect on bandwidth, but for maximum isolation the R_{ON} value must be low (50Ω or less).

(Circle 1)

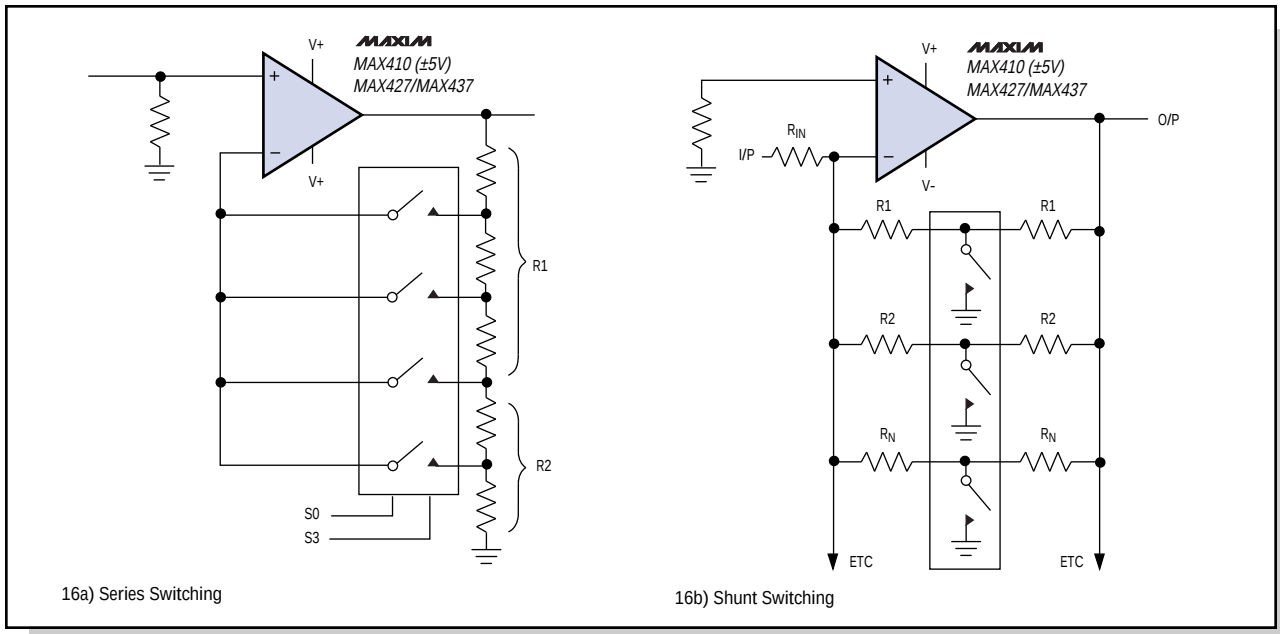


*Figure 16. Gain-control circuits can employ series (**a**) or shunt (**b**) switching.*

SELECTION GUIDES

FAULT PROTECTION

Device	Industry Cross	Function (Mux)	Latched Inputs	Fault Protection (V)	Price* ($)
MAX354	ADG508F			±40	2.45
MAX355	ADG509F			±40	2.45
MAX358	DG508A**/HI508A	8:1	–	±35	2.45
MAX359	DG509A**/HI509A	4:2 Diff	–	±35	2.45
MAX368	DG528**/ADG529**	8:1	Yes	±35	3.50
MAX369	DG529**/ADG529**	4:2 Diff	Yes	±35	3.50
MAX378	HI548	8:1	–	±75	3.50
MAX379	HI549	4:2 Diff	–	±75	3.50
MAX388	DG528**	8:1	Yes	±100	4.50
MAX389	DG528**	4:2 Diff	Yes	±100	4.50

* Prices are 1000 pc., FOB USA
** Requires external components for protection

ULTRA-LOW LEAKAGE

Device	Function	Industry Cross	Off Leakage (pA max)	RON (Ω max)	Charge Injection (pC)
MAX326	Quad SPST	DG201	10	2.5k	3 (typ)
MAX327	Quad SPST	DG202	10	2.5k	3 (typ)
MAX328	8-Ch Mux	DG508A	10	2.5k	3 (typ)
MAX329	Dual 4-Ch Mux	DG509A	10	2.5k	3 (typ)
MAX338	8-Ch Mux	DG508A	20	400	5 (max)
MAX339	Dual 4-Ch Mux	DG509A	20	400	5 (max)

SELECTION GUIDES (continued)

LOW ON-RESISTANCE

Device	Function	On-Resistance (Ω max)	R_{ON} Match (Ω max)			R_{ON} Flatness (Ω max)			Charge Injection (pC max)		
			BEST	BETTER	OK	BEST	BETTER	OK	BEST	BETTER	OK
MAX301/DG401	Dual SPST	35	2	2	3	Δ3	Δ3	NT	15	15	NT
MAX303/DG403	Dual SPDT	35	2	2	3	Δ3	Δ3	NT	15	15	NT
MAX305/DG405	Dual DPST	35	2	2	3	Δ3	Δ3	NT	15	15	NT
MAX306/DG406	16-Ch Mux	100	5	10	NT	Δ7	Δ10	NT	10	10	NT
MAX307/DG407	Dual 8-Ch Mux	100	5	10	NT	Δ7	Δ10	NT	10	10	NT
MAX308/DG408	8-Ch Mux	100	5	10	15	Δ7	Δ10	NT	10	10	NT
MAX309/DG409	Dual 4-Ch Mux	100	5	10	15	Δ7	Δ10	NT	10	10	NT
MAX312/DG411	Quad SPST	10	1.5	–	NT	Δ2	–	NT	30	–	NT
MAX313/DG412	Quad SPST	10	1.5	–	NT	Δ2	–	NT	30	–	NT
MAX314/DG413	Quad SPST	10	1.5	–	NT	Δ2	–	NT	30	–	NT
MAX351/DG411	Quad SPST	35	2	3	NT	Δ3	Δ4	NT	10	10	NT
MAX352/DG412	Quad SPST	35	2	3	NT	Δ3	Δ4	NT	10	10	NT
MAX353/DG413	Quad SPST	35	2	3	NT	Δ3	Δ4	NT	10	10	NT
MAX317/DG417	SPST	35	N/A	N/A	NT	Δ3	Δ4	NT	10	10	NT
MAX318/DG418	SPST	35	N/A	N/A	NT	Δ3	Δ4	NT	10	10	NT
MAX319/DG419	SPDT	35	2	3	NT	Δ3	Δ4	NT	10	10	NT
DG421	Dual SPST*	35	N/A	3	NT	N/A	Δ4	NT	N/A	15	NT
DG423	Dual SPDT*	35	N/A	3	NT	N/A	Δ4	NT	N/A	15	NT
DG425	Dual DPST*	35	N/A	3	NT	N/A	Δ4	NT	N/A	15	NT
MAX361/DG441	Quad SPST	85	2	4	NT	Δ5	Δ9	NT	5	10	NT
MAX362/DG442	Quad SPST	85	2	4	NT	Δ5	Δ9	NT	5	10	NT
MAX364/DG444	Quad SPST	85	2	4	NT	Δ5	Δ9	NT	5	10	NT
MAX365/DG445	Quad SPST	85	2	4	NT	Δ5	Δ9	NT	5	10	NT

Best = MAX3xx
Better = Maxim's Improved DG4xx
OK = Competitive Industry Standard

* Latched address inputs
NT = Not Tested

LOW VOLTAGE (2.7V to 16V)

	DEVICE	FUNCTION	ON-RESISTANCE MATCH (Ω max)	ON-RESISTANCE FLATNESS (Ω max)	CHARGE INJECTION (pC max)	PIN COMPATIBLE	µMAX PACKAGE
	SWITCHES						
	MAX320	Dual SPST (NO)	2	6	5	TSCW66F	✔
	MAX321	Dual SPST (NC)	2	6	5	TSCW66F	✔
	MAX322	Dual SPST (NO, NC)	2	6	5	TSCW66F	✔
	MAX323	Dual SPST (NO)	2	6	5	TSCW66F	✔
	MAX324	Dual SPST (NC)	2	6	5	TSCW66F	✔
	MAX325	Dual SPST (NO, NC)	2	6	5	TSCW66F	✔
	MAX381	Dual SPST (NO)	2	6	5	DG401	
	MAX383	Dual SPDT	2	6	5	DG403	
	MAX385	Dual DPST (NO)	2	6	5	DG405	
	MAX391	Quad SPST (NC)	2	6	5	DG411	
	MAX392	Quad SPST (NO)	2	6	5	DG412	
	MAX393	Quad SPST (NO, NC)	2	6	5	DG413	
	MAX394	Quad SPDT	2	6	5	MAX333	
NEW	MAX4066/A	Quad SPST	2	6	10	74HC4066	QSOP
	DEVICE	FUNCTION	ON-RESISTANCE MATCH (Ω max)	ON-RESISTANCE FLATNESS (Ω max)	CHARGE INJECTION (pC max)	PIN COMPATIBLE	LATCHED INPUT
	MUXES						
	MAX382	8-Channel Mux	10	16	5	DG428	✔
	MAX384	Dual 4-Channel Mux	10	16	5	DG429	✔
	MAX395†	8-Channel Mux	10	16	5	MAX335	SERIAL CONTROL
	MAX396	16-Channel Mux	10	16	5	DG406	
	MAX397	Dual 8-Channel Mux	10	16	5	DG407	
	MAX398	8-Channel Mux	10	16	5	DG408	
	MAX399	Dual 4-Channel Mux	10	16	5	DG409	
NEW	MAX4051/A†	8-Channel Mux	15	16	10	74HC4051	
NEW	MAX4052/A†	Dual 4-Channel Mux	15	16	10	74HC4052	
NEW	MAX4053/A†	Triple 2-Channel Mux	15	16	10	74HC4053	

† Future Product—available after November 1995

PC printer port controls data logger

Engineering projects often require measurements over an extended period of time. A commercial data logger or pen plotter will do the job, but those instruments are expensive. As an inexpensive alternative (**Figure 1**), you can combine a simple, 4-channel data-acquisition circuit with a tool available to most engineers: the personal computer or PC. The PC also lets you manipulate data in spreadsheets and incorporate it into reports.

One of the computer's printer ports controls the data logger and provides 5V power. Five volts also powers the charge-pump voltage inverter (IC1) that produces a local -5V supply. The negative supply current is small, so simple RC filters at IC2 and IC4 are adequate for reducing the charge pump's switching noise. (Similar filters on the 5V supply reduce the effect of noise from the PC.) This circuit draws only 220µA.

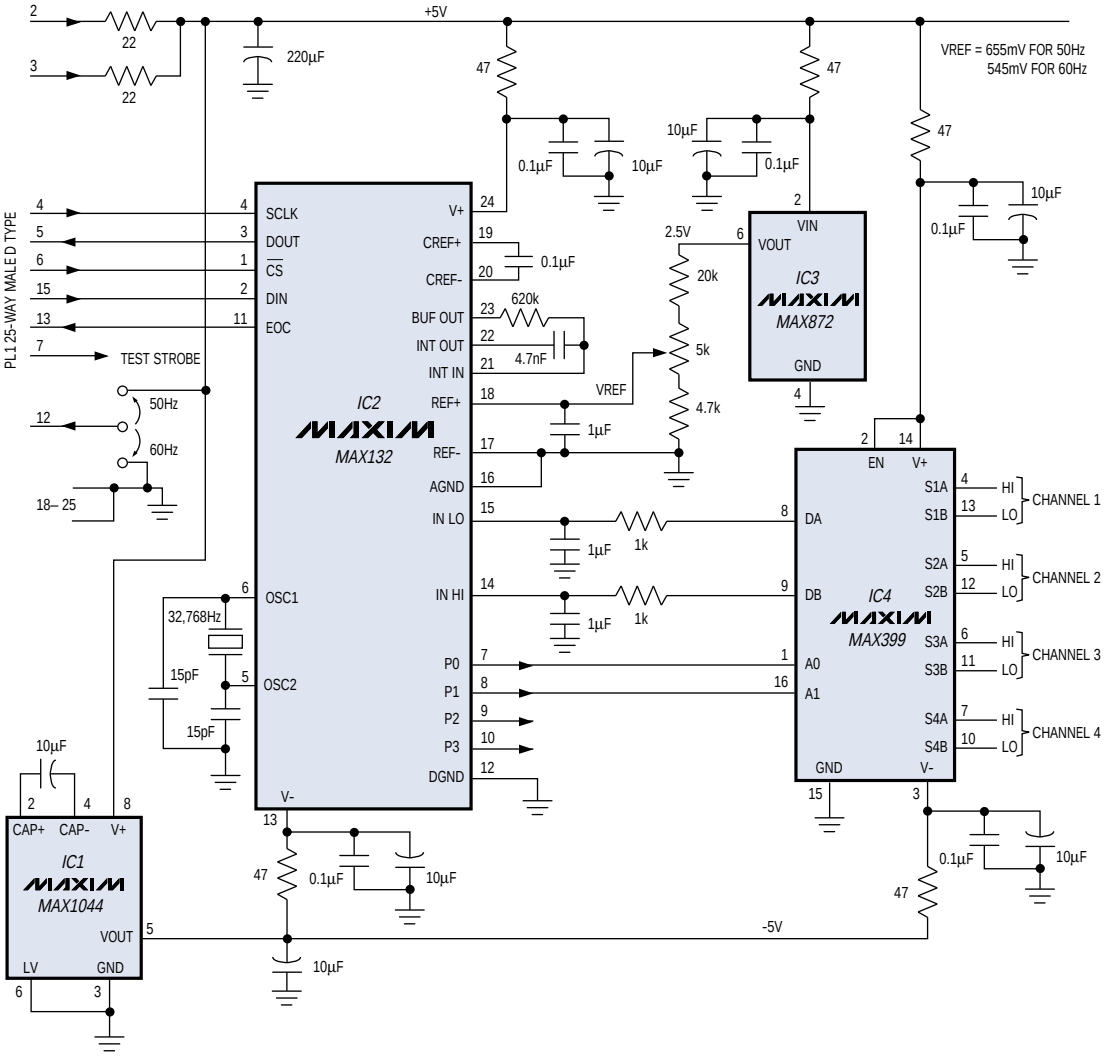


Figure 1. This 4-channel data logger obtains power and control signals through the printer port of a PC. The PC can present the data as a plot or a list, or route it to a file for later analysis.

A QBASIC program (available from Maxim) lets the system sample and display as many as four channels, both as present readings and as plots with time indicators (**Figure 2**). Or it can write the data to a file for later evaluation. QBASIC is available with MS-DOS on most PCs. Though fairly slow, it easily accommodates different tasks, more channels, different scaling, etc., and makes data calculations such as the minimum, maximum, and average. Minimum cycle time for reading the four channels is one second, and the graphics output is scaled for a VGA monitor with 640 x 480 resolution.

The A/D converter is a 15-bit multi-slope device (MAX132), which (in this application) gives a resolution of about 15µV. It includes a serial interface for data and control signals, and four digital outputs (P0–P3) for controlling multiplexers and other peripherals.

IC2 provides a reference voltage of 2.5V, scaled as required to optimize line-frequency rejection in the A/D converter: 655mV for 50Hz lines, or 545mV for 60Hz lines. Software senses the state of pin 12 in the printer connector (jumpered as shown for a 50Hz or 60Hz line frequency) and adjusts the A/D converter's integration time accordingly.

The TEST STROBE is a pulse at the start of each set of readings. Present on pin 7 of the 25-pin printer connector, it simplifies debug and troubleshooting operations by serving as a trigger for the oscilloscope.

(Circle 2)

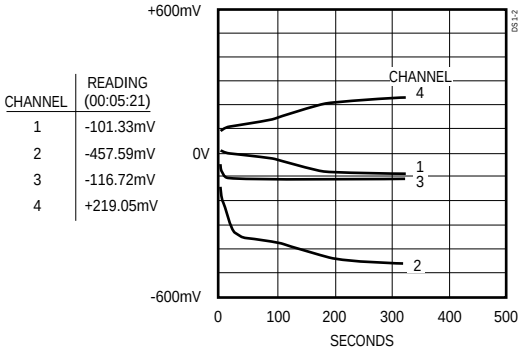


Figure 2. The program output can track four channels as shown.

DC-DC controller drives regulated charge pump

A switch-mode power-supply controller and diode-capacitor network can generate the modest negative supply currents required for op amps or for LCD bias, without the design effort and size penalty associated with inductors (**Figure 1**). The circuit of Figure 1 accepts inputs of 2V to 6V and produces a digitally adjustable output voltage. The diode-capacitor charge pump is driven by the switching action of DHI and DLOW, which normally drive an external MOSFET or pnp transistor in an inductor-based switch-mode power supply.

At power-up, the internal 6-bit current-output D/A converter produces a nominal V_{OUT} of R1 x 13.33µA. Then, by holding CTRL high and toggling ADJ, you can adjust V_{OUT} over a 3:1 range in 64 equal steps, according to the value of R1: R1 x 6.66µA ≤ V_{OUT} ≤ R1 x 20µA. If digital adjustment is not required, ground the ADJ pin and connect CTRL to V+. Or construct a similar circuit with the MAX774 dc-dc controller, which accepts inputs up to 16.5V. For positive outputs greater than V_{IN}, a step-up controller and modified charge-pump network (not shown) can do the job.

The maximum output current depends on V_{IN}, V_{OUT}, and the number of diode-capacitor stages, each of which consists of two diodes and two capacitors. Though only a few microamps are available at the maximum V_{OUT}, which equals V_{IN} - (0.6V x the number of stages), you can draw more current at the lower output voltages (**Figure 2**).

The number of diode-capacitor stages determines the maximum I_{OUT} for a given V_{IN} and V_{OUT}. Too few stages will not achieve the desired voltage, but too many degrades the efficiency: I_{IN} equals (approximately) I_{OUT} times the number of stages. For V_{IN} less than 5V, the circuit delivers less output current than is indicated by the curves of Figure 2. For example, a 4-stage circuit produces an output current

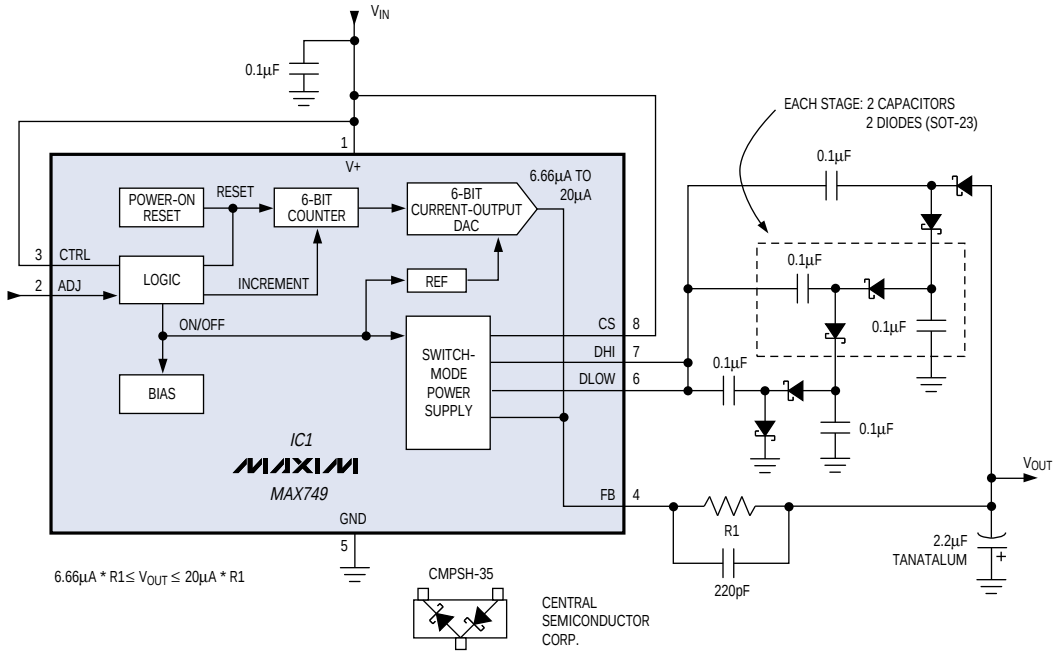


Figure 1. Driving a diode-capacitor network instead of an inductor, this dc-dc controller IC produces a regulated negative output with modest I_{OUT} capability.

of 1mA at -2V out from 2V in, at -7V from 3V in, at -11V from 4V in, and at -14.5V from 5V in. Larger pump capacitors can provide higher I_{OUT}.

The controller changes its behavior when V_{OUT} is much lower than the voltage programmed by R1. Designed for inductor-based circuits, it compensates for impending dropout by increasing the switching transistor's "on" time at the expense of "off" time. This action normally ramps up the inductor current, but it has an opposite effect for the circuit shown. Because short off times (DHI high) don't allow the capacitors to discharge fully, the available output current actually decreases instead of increasing. Thus, when V_{OUT} loses regulation due to overload, you must reduce the load current considerably before regulation can be regained. A reliable maximum output current is the level at which V_{OUT} recovers from dropout, not the higher level at which it enters dropout.

For stable operation, bypass R1 with 220pF, keep the connections between R1 and IC1 very short, and place the input bypass capacitor directly across the input pins of IC1. Output ripple is typically less than 1% for the component values shown, but ripple can be higher if the circuit includes more stages than that required by the programmed output voltage. Ripple can be lowered by increasing the output capacitance.

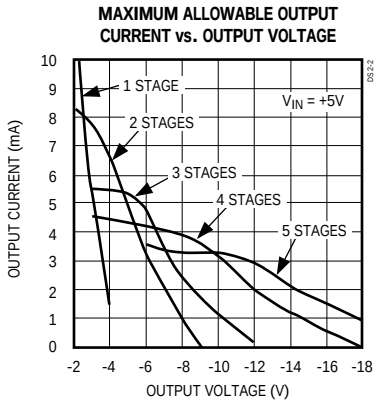


Figure 2. The available output current in Figure 1 depends on V_{IN} (5V for this graph), V_{OUT}, and the number of diode-capacitor stages.

(Circle 3)

Circuit guards battery against polarity reversal and high current

The **Figure 1** circuit protects a battery-operated system in two ways: Q1 prevents damage due to the flow of reverse current that otherwise occurs when the battery is installed backward, and Q3 prevents the excessive flow that otherwise occurs with a sudden load increase or short circuit.

A properly installed battery fully enhances Q1 by pulling its gate more than 5V below the source. If the battery is installed backward, Q1 is off because the gate is positive with respect to the source. Regardless of battery polarity, the body diodes of Q1 and Q3 are oriented to ensure that no current can flow when either device is off. Both FETs have low on-resistance.

IC2 is a current-sense amplifier that senses the load current flowing between its RS+ and RS- terminals. Its output is a proportional but smaller current at OUT (1.5mA maximum), which develops a voltage across R8 proportional to the load current. During normal operation, both comparator outputs are high and Q3 remains on.

When the load current exceeds a limit set by R8, (i.e. $I_{LIMIT} = 2000V_{TH} / R8$, where 2000 is the sense amplifier's gain and V_{TH} is the comparators' input threshold (1.182V ±2%), the B comparator output goes low and turns off Q4, which turns off Q3 and disconnects the battery from its load. At the same time, Q6 provides positive feedback by pulling the comparator input up to the collapsing supply rail, latching Q3 off as the supply voltage drops.

An output short circuit turns off IC2 by removing the voltage at pins 6 and 7. Three volts is the minimum for proper operation. Control via the B comparator is lost because the R8 voltage goes to zero for this short-circuit condition, but comparator A then shuts off Q3 by turning off Q5. Q2 speeds the Q3 turn-off time to about 10µs.

When Q3 is off, the circuit draws about 2µA. (To restore power, you press S1.) During normal operation, the battery current varies with its terminal voltage: 200µA at 5V, 230µA at 6V, 300µA at 8V, and 310µA at 10V.

(Circle 4)

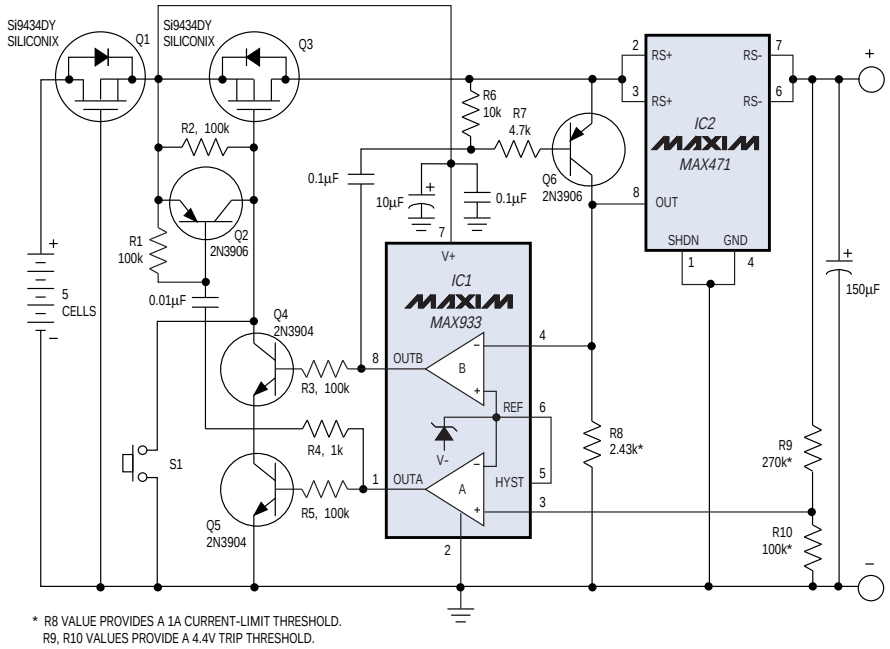


Figure 1. This load-protection circuit prevents current flow in response to excessive loads, output short circuits, and wrong-polarity connections to the battery.

Battery charger indicates trickle or fast charge

A single LED indicates whether the battery charger of **Figure 1** is delivering a fast charge or a trickle charge. During fast charges, the LED lights continuously because IC2's $\overline{\text{FASTCH}}$ output sinks dc current. During trickle charges, it flashes because D1 and Q1 enable the 555 timer.

The timer is configured as an astable multivibrator operating at 60Hz (f = 1 / 1.4RC). It remains enabled during a fast charge, but must shut off when the battery is disconnected. Zener diode D1 makes that decision. With no battery connected (a condition sensed by R5 and an internal comparator), IC2 produces a voltage at BATT+ equal to twice the number of cells for which the IC is programmed. This voltage (4V for two cells) turns on the 3.3V zener and disables the timer.

Connecting a battery drops the BATT+ voltage to 2.8V (1.4V per cell), which turns off D1, turns off Q1, and enables the timer. The timer output drives Q3, whose collector (wire-OR'd with the open-drain $\overline{\text{FASTCH}}$ output) causes the LED to flash.

Other cell counts require different zener voltages:

Cell Count	BATT+ Voltage (V)	Charged-Battery Voltage (V)	Required Zener Voltage (V)
2	4	2.8	3.3
4	8	5.6	6.8
6	12	8.4	10
8	16	11.2	15
10	20	14	18
12	24	16.8	18
14	28	19.6	24

During a fast charge, the LED should glow steadily, without flicker caused by the operating timer. This condition is assured if the $\overline{\text{FASTCH}}$ voltage remains low: IC2's data sheet guarantees a 0.4V maximum when $\overline{\text{FASTCH}}$ sinks 2mA. Higher currents produce a higher voltage that may result in flicker. In that case, you can cure the problem by adding a resistor in the emitter of Q3.

(Circle 5)

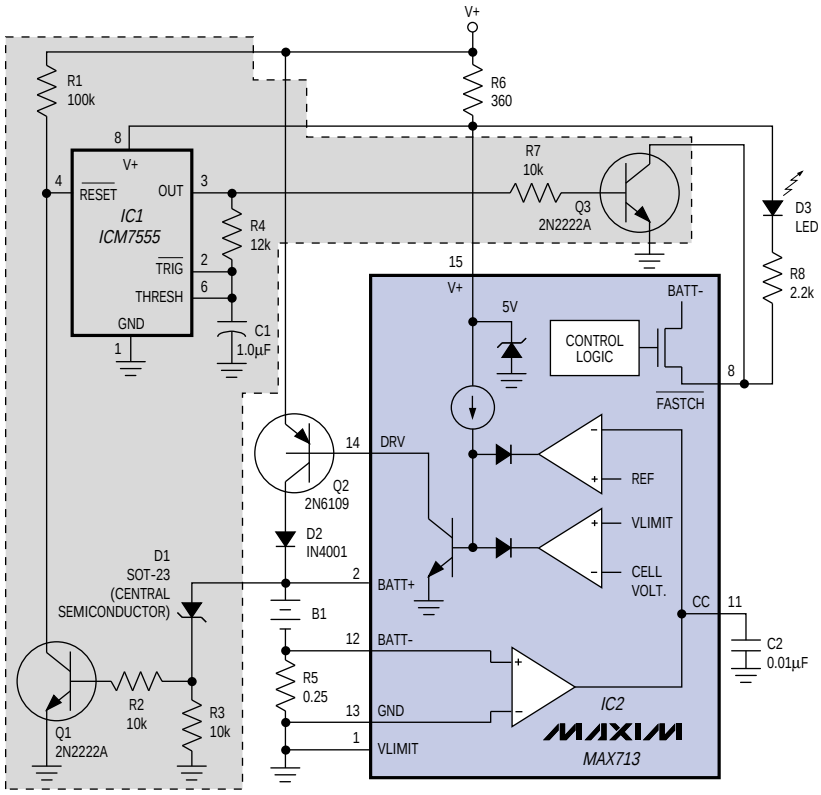


Figure 1. The shaded components in this NiCd (or NiMH) battery charger cause the LED to flash during trickle charges.

Switch allows low-voltage regulator to start under load

The addition of an external load-disconnect switch allows a CMOS switching regulator to start with load currents several decades higher than otherwise possible (**Figure 1**). CMOS regulators are excellent for portable applications because they have very low operating and shutdown currents (IC1 operates on 25µA and shuts down to 1µA), and they provide ample current once started. But many cannot start *under maximum load* from low supply voltages such as those provided by single-cell batteries.

The problem arises because most low-voltage CMOS boost regulators are powered from their own output, which equals V_{IN} minus a diode drop at start-up. Low values of input voltage don't allow the switching transistor to become fully enhanced, so it presents a high impedance that limits the peak inductor current. As a result, the circuit cannot produce enough current to supply the load and charge the output capacitor at the same time.

You can overcome this start-up limitation with an external power MOSFET, operating in conjunction with the low-battery comparator built into many low-voltage switching regulators. Acting as a load switch, Q1 disconnects the load until V_{OUT} is high enough to fully enhance N1. The circuit can then start with much higher values of I_{LOAD} (**Figure 2**). With the load switch in place, the circuit can start under full load with input voltages as low as 0.8V.

Q1 as shown is a low-threshold power MOSFET. Because the regulator's feedback is taken before this switch, the device chosen in a given application depends on the load current and the minimum level of load regulation acceptable. Results similar to those of Figure 2 apply for a 5V regulated output, which is obtained by connecting the $3/\overline{5}$ terminal (pin 2) to ground.

(Circle 6)

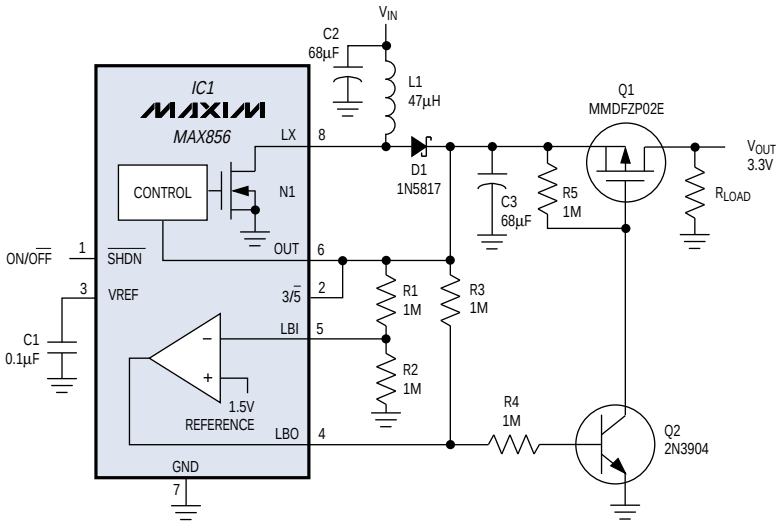


Figure 1. Load-disconnect switch Q1 allows this CMOS switching regulator to start, under load, from very low input voltages.

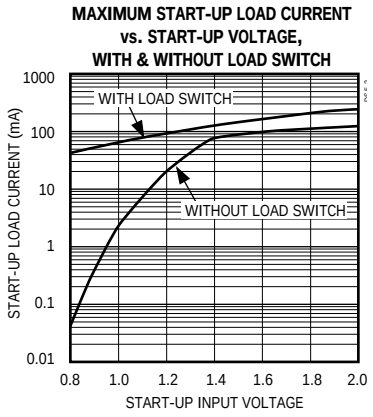


Figure 2. These curves show the highest load current permissible in the Figure 1 circuit for a given input voltage at start-up. The load switch permits several decades more load current at low input voltages.

NEW PRODUCTS

Full-function µP supervisor has ±1.5% reset accuracy

MAX807 microprocessor supervisors reduce a design risk inherent in the V_{CC}-monitor function: an IC can be forced to operate between its minimum operating voltage and a somewhat lower minimum specified for the reset trip threshold. A tight tolerance of ±1.5% on the MAX807's reset trip threshold reduces this unspecified operating range by 40%.

Consider, for example, a system specified for V_{CC} ±10% in which the ICs are guaranteed only for V_{CC} ±5%. Reset should occur at 4.75V but no higher, so a practical reset range must extend downward—to 4.5V, for example. In that case, some systems will operate their ICs in the unspecified range between 4.5V and 4.75V. (Designers often produce such systems, knowing that most ICs can operate below their specified supply level, and that actual reset thresholds seldom approach the specified minimum.) Tightening the µP supervisor's reset-threshold tolerance shrinks this unspecified range by raising the minimum reset threshold.

RESET (and $\overline{\text{RESET}}$) are asserted during conditions of power-up, power-down, and brownout—whenever V_{CC} dips below the threshold level. Reset thresholds are accurate to within ±1.5%: 4.75V to 4.6V (L suffix), 4.5V to 4.35V (M), and 4.65V to 4.5V (N). Correct resets are guaranteed for V_{CC} as low as 1V. Resets can also be triggered manually by applying a low logic level at the $\overline{\text{MR}}$ input. A separate low-line comparator provides an early power-fail warning by comparing V_{CC} to a threshold 30mV above the reset threshold. The result is a two-stage warning in which both are more accurate than those of earlier µP supervisors.

The MAX807's 7ns propagation delay for chip-enable signals makes it suitable for high-performance equipment, as does its output-current capability (250mA in normal operation, 20mA in backup). On the other hand, its 70µA supply current is ideal for portable systems. Standby current is only 1µA.

The MAX807 includes other housekeeping functions: switchover circuitry transfers low-power loads (CMOS RAM, real-time clocks, and other low-power logic) from V_{CC} to the backup battery. A write-protect signal guards CMOS RAM and EEPROM memories by preventing write operations during conditions of low V_{CC}. And, a watchdog circuit issues a warning ($\overline{\text{WDO}}$ low) whenever software execution fails to toggle a selected line within the timeout period.

The MAX807 comes in 16-pin DIP and wide-SO packages, in versions tested for the commercial (0°C to +70°C), extended-industrial (-40°C to +85°C), and military (-55°C to +125°C) temperature ranges. Prices start at $3.21 (1000 up, FOB USA).

(Circle 7)

8-pin op-amp/ comparator/ reference IC draws 7µA from single supply

MAX951–MAX954 ICs are ideal for use in bar-code readers, photodiode preamplifiers, low-frequency local-area alarms and detectors, and other low-power, battery-operated systems. The MAX951 and MAX952 operate down to 2.8V. Both include an op amp and comparator whose negative input is connected to a 1.2V ±2% bandgap reference. The similar MAX953 and MAX954 require an external reference but have identical 8-lead pinouts.

The MAX951 and MAX953 op amps are unity-gain stable; MAX952 and MAX954 op amps must operate with a minimum gain of ten. All have unusual output stages that enable linear operation under load and with ultra-low supply currents: 7µA for the MAX951/MAX953 and 5µA for the MAX952/MAX954. The op amps minimize output error by maintaining good dc characteristics over the entire operating temperature range. Outputs swing rail-to-rail.

The common-mode input range for the op amps and comparators extends from the negative rail to within 1.3V of the positive rail. The comparator output stages can deliver 40mA continuously or 100mA in short pulses, and the comparators' ±3mV internal hysteresis ensures clean output switching even with slow-moving input signals. In addition, the comparators produce no power-supply glitches (crowbar glitches) when changing logic states. The result is twofold: immunity to instability caused by parasitic feedback, and excellent performance even with non-optimal circuit layouts.

MAX951–MAX954 devices come in 8-pin DIP, SO, and µMAX packages, in versions tested for the extended-industrial (-40°C to +85°C) and military (-55°C to +125°C) temperature ranges. Prices start at $1.60 (1000 up, FOB USA).

(Circle 8)

500MHz, voltage-feedback video op amps draw only 5mA

MAX4100/MAX4101 voltage-feedback op amps are the first amplifiers designed in Maxim's proprietary, complementary, 9.3GHz fabrication process. Compensated for closed-loop gains (A_{VCL}) of 1 and 2 respectively, they draw only 5mA from ±5V supplies. Yet the robust output stage delivers 80mA output currents and swings ±3.3V into 100Ω.

Low power and high speed (the MAX4100's -3dB bandwidth is 500MHz) make the op amps suitable for portable instrumentation and multichannel applications in which power consumption is critical, such as video, medical imaging, and telecommunications. Voltage feedback lets you configure the op amps as traditional inverting or noninverting gain blocks, while providing low offset voltage and a balanced input stage with low input bias current.

MAX4100/MAX4101 ac performance includes a 250V/µs slew rate, 0.1dB gain flatness to 65MHz, a -70dBc spurious-free dynamic range (SFDR) with f_C = 5MHz, 12ns settling time to ±0.1%, and low differential gain and phase errors. The combination of speed and low distortion opens a wide range of applications for the MAX4100 and MAX4101, including use as an input buffer for A/D converters.

MAX4100/MAX4101 devices come in 8-pin SO packages tested for the extended-industrial (-40°C to +85°C) temperature range. Prices start at $1.95 (1000 up, FOB USA).

(Circle 9)

NEW PRODUCTS

330MHz video crosspoint ICs offer 0.01°/0.01% accuracy

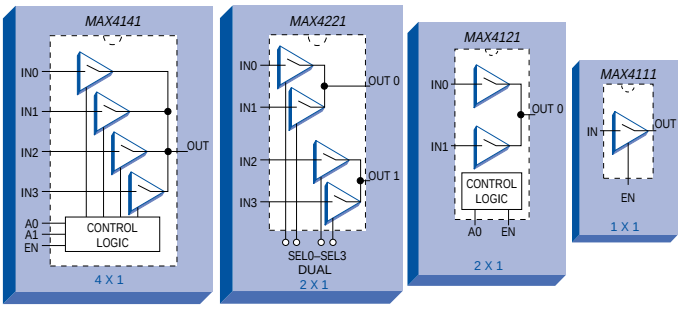
The MAX4111, MAX4121, MAX4221, and MAX4141 are building-block ICs for video crosspoint systems. They operate on ±5V and draw only 5.5mA. The MAX4111 is an SPST switch, the MAX4121 is an SPDT switch, the MAX4221 is a dual SPDT switch, and the MAX4141 is a 4-channel, single-ended multiplexer. Their primary application is the color-signal multiplexing of broadcast-quality composite video in NTSC, PAL, SECAM, and HDTV systems; they're also suitable for routing RF, IF, video, and telecom signals.

Each signal channel includes an open-loop output buffer with high input impedance, 0.1dB gain flatness to 150MHz, a -3dB bandwidth of 330MHz, and the capability to drive large capacitive loads. All four ICs provide low differential phase/gain errors of only 0.01°/0.01%, and an ultra-low (<13mV) switching transient that is always positive to avoid corrupting the negative-going sync pulses.

Each IC has an enable (EN) input that forces each output to a high-impedance state and lowers the supply current to only 250µA. MAX4141 and MAX4221 devices save external components by integrating the necessary control logic on chip. At 30MHz, the MAX4121 exhibits -92dB crosstalk and -78dB off isolation.

The MAX4111 and MAX4121 come in an 8-pin SO package, the MAX4221 comes in a 16-pin narrow SO, and the MAX4141 comes in a 14-pin SO. All are tested for the commercial (0°C to +70°C) temperature range. Prices start at $1.70 for the MAX4111 (1000 up, FOB USA).

(Circle 10)



16-channel multiplexers operate on 2.7V

The 16-channel MAX396 and the dual 4-channel MAX397 are CMOS analog multiplexers that operate on supply voltages as low as 2.7V. Each operates from +2.7V to +16.5V or from ±2.7V to ±8V, while retaining CMOS-logic compatibility and fast switching (250ns transition times). On-resistances (only 100Ω maximum) are matched to within 4Ω maximum between channels and are flat to within 10Ω maximum over the specified signal range.

Each device features low leakage over temperature: at +85°C, the output off leakage is 2.5nA and the input off leakage is 1nA. Each device is fabricated in Maxim's low-voltage silicon-gate process and offers design improvements that ensure extremely low values of charge injection (5pC maximum). Improvements also guarantee protection to 2000V against electrostatic discharge (ESD) per MIL-STD-883, Method 3015.7. Power consumption is only 10µW.

MAX396/MAX397 multiplexers are pin compatible with the industry-standard MAX306/MAX307, DG406/DG407, and DG506A/DG507A. They come in 28-pin DIP, SO, and wide-SSOP packages, in versions tested for the the commercial (0°C to +70°C), extended-industrial (-40°C to +85°C), and military (-55°C to +125°C) temperature ranges. Prices start at $4.04 (1000 up, FOB USA).

(Circle 11)

5A step-down converters provide 5V, 3.3V, and 3V outputs

The MAX787, MAX788*, and MAX789* switch-mode dc-dc regulators employ pulse-width-modulation (PWM) in a classic buck-regulator topology. Each monolithic, bipolar device includes a 5A power switch and is capable of delivering continuous load currents as high as 5A. The output voltages are 5V (MAX787), 3.3V (MAX788), and 3V (MAX789).

High operating frequencies (100kHz) enable each regulator to operate with a small external inductor, Schottky diode, and output filter capacitor. Few external components are required because the oscillator, power switch, and control circuitry are all on-chip. Supply current is 8.5mA for each regulator.

Each device has an input-voltage range of 8V to 40V. Cycle-by-cycle current limiting (preset to 6.5A) protects the output against overcurrent and short-circuit faults. Excellent dynamic characteristics provide a well-behaved transient response.

MAX787/MAX788/MAX789 devices come in 5-pin TO-220 packages, in versions tested for the commercial (0°C to +70°C) and extended-industrial (-40°C to +85°C) temperature ranges. Prices start at $4.52 (1000 up, FOB USA).

(Circle 12)

CLOSELY RELATED PRODUCTS

	Maximum Output Current		
VOUT	5A (TO-220)	2A (TO-220)	1A (16-pin SOIC)
5V	MAX787	MAX727	MAX831
3.3V	MAX788*	MAX728	MAX832*
3V	MAX789*	MAX729	MAX833*
Adjustable	MAX724	MAX726	MAX830

* Future Product—contact factory for availability.

NEW PRODUCTS

5V step-down regulators come in 16-pin SOICs

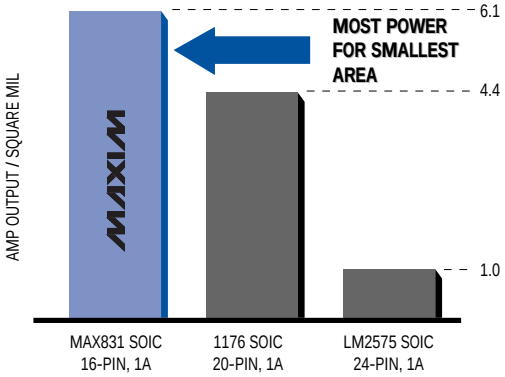
The MAX830–MAX833 switch-mode, step-down dc-dc regulators produce fixed outputs for an input of 8V to 30V. MAX831/MAX832*/MAX833* outputs are 5V/3.3V/3.0V respectively, and the MAX830 output is adjustable. Each device is rated at 1A for continuous output current. The power switch, oscillator, and feedback/control circuitry are all on-chip, so complete circuits require only six external components.

Each device has a 100kHz preset frequency for the internal oscillator. Quiescent current is 8mA, falling to 500µA (maximum) in the digitally controlled shutdown mode. Maximum switch current is controlled by an external resistor. Each regulator has excellent dynamic characteristics that provide a well-behaved transient response, and cycle-by-cycle current limiting to protect against overcurrent and short-circuit-output faults.

MAX830–MAX833 devices come in 16-pin wide-SO packages, tested for the commercial (0°C to +70°C) temperature range. Prices start at $3.99 (1000 up, FOB USA). An evaluation kit (MAX831EVKIT-SO) is available to speed and simplify your design cycle.

* Future Product—contact factory for availability.

(Circle 13)



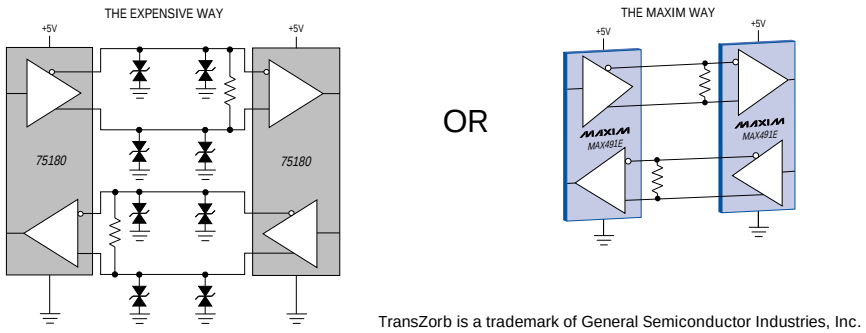
RS-485/RS-422 transceivers withstand ±15kV ESD

The MAX491E data transceiver operates on 5V and contains one driver and one receiver, enabling full-duplex communications on RS-485 and RS-422 transmission lines. Proprietary internal structures protect the device against electrostatic discharge (ESD) as high as ±15kV, without latchup. The internal structures also obviate the need for expensive TransZorb™ protection.

One of a family of RS-485/RS-422 transceivers, the MAX491E has a driver output with nonlimited slew rate, which enables data rates to 2.5Mbps. The driver output is also current limited against short circuits, and protected against excessive power dissipation by thermal-shutdown circuitry that places the output in a high-impedance state. The receiver guarantees a high output level when its input is open-circuited.

The MAX491E features a 30ns propagation delay and 5ns differential receiver skew. It has separate driver and receiver enables, and allows as many as 32 transceivers on one bus. The MAX491E comes in 14-pin DIP and SO packages, in versions tested for the commercial (0°C to +70°C) and extended-industrial (-40°C to +85°C) temperature ranges. Prices start at $1.50 (1000 up, FOB USA).

(Circle 14)



TransZorb is a trademark of General Semiconductor Industries, Inc.

Quad RS-232 line driver and receiver withstand ±15kV ESD

The MAX1488E quad driver and MAX1489E quad receiver are designed for EIA/TIA-232, EIA/TIA-562, and CCITT V.28 communications in harsh environments. Each driver output and receiver input is protected against electrostatic-discharge (ESD) levels as high as ±15kV. Both devices are free of latchup, even during an ESD event. ESD ratings are as follows:

MAX1488E
±15kV— Human Body Model
±6kV— IEC801-2, Contact Discharge
±15kV— IEC801-2, Air-Gap Discharge
MAX1489E
±15kV— Human Body Model
±8kV— IEC1000-4-2, Contact Discharge
±15kV— IEC1000-4-2, Air-Gap Discharge

Both devices guarantee a maximum data rate of 120kbps. The driver outputs feature slew-rate limiting and current limiting that is internally controlled, so no external capacitors are required. Receiver inputs feature a ±25V range, with hysteresis and time-domain filtering that eliminate the need for an external filter. The receiver outputs are TTL and CMOS compatible.

The MAX1488E operates from ±4.5V to ±13.2V and draws only 85µA from each rail. It is pin compatible with the MC1488, MC14C88, SN75188, SN75C188, DS1488, and DS14C88. The MAX1489E operates on 5V ±10%, draws 350µA, and is pin compatible with the MC1489, MC14C89, SN75189, DS1489, and DS14C89.

MAX1488E/MAX1489E devices come in 14-pin DIP and SO packages, in versions tested for the commercial (0°C to +70°C) and extended-industrial (-40°C to +85°C) temperature ranges. Prices start at $0.95 (1000 up, FOB USA).

(Circle 15)